CLAIMS

What is claimed is:

1. A calibration circuit capable of calibrating an electronic device while the input of the electronic device is coupled to a signal source, the calibration circuit comprising:

a calibration excitation signal generator configured to generate a calibration excitation signal coupled to a signal path of the electronic device;

a calibration error signal detector configured to receive an error signal from the signal path of the electronic device while the signal path of the electronic device is coupled to a normal operating signal source; and

a variable transfer function circuit element in the signal path, the variable circuit element having a transfer function which is variable in response to a signal from the calibration error signal detector.

2. The calibration circuit of claim 1, wherein the variable transfer function circuit element comprises at least one of a variable resistor, a variable capacitor, and a variable current mirror.

3. The calibration circuit of claim 1, wherein the calibration excitation signal generator is configured to generate a signal at an out-of-band frequency.

4. The calibration circuit of claim 3, wherein the calibration excitation signal generator further comprises a switch configured to toggle between first and second reference voltages in response to a clock signal.

5. The calibration circuit of claim 1, wherein the calibration excitation signal generator is configured to generate a calibration excitation signal having a shaped frequency spectrum.

6. The calibration circuit of claim 5, wherein the shaped frequency spectrum is one of random and pseudo random shaping.

7. The calibration circuit of claim 1, wherein the calibration error signal detector comprises a synchronous error detector.

8. The calibration circuit of claim 7, wherein the synchronous error detector comprises:

a latched comparator having first and second inputs and an output;

a capacitor having a first terminal coupled to the first input of the latched comparator and a second terminal for coupling to the output of the electronic device; and

a switch coupled to the first terminal of the capacitor for selectively switching the first terminal of the capacitor to a reference voltage.

9. The calibration circuit of claim 7, wherein the calibration error signal detector further comprises a calibration loop filter coupled between an output of the synchronous error detector and an input of the variable transfer function circuit element.

10. The calibration circuit of claim 9, wherein the calibration loop compensation comprises an up/down counter.

11. The calibration circuit of claim 1, wherein at least one of the calibration error signal detector and the calibration excitation signal generator is configured to operate in accordance with one of a random clock signal, a pseudo-random clock signal, an out-of-band clock signal and a frequency spectrum shaped signal.

12. The calibration circuit of claim 1, wherein the electronic device is configured as a difference amplifier.

13. An electronic circuit having a signal path coupled to receive an operating signal, the electronic circuit producing an output in response to the operating signal, the electronic circuit comprising:

a calibration excitation signal generator configured to generate a calibration excitation signal;

a variable transfer function circuit element coupled between the calibration excitation signal generator and the signal path of the electronic circuit, the electronic circuit producing on its signal path a calibration error signal superimposed on the operating signal in response to the calibration excitation signal;

a calibration error signal detector coupled to the signal path of the electronic circuit for detecting the calibration error signal during normal operation of the electronic circuit; and

a filter circuit coupled between the calibration error signal detector and the variable transfer function circuit element, wherein the filter circuit is configured to generate an adjustment signal operative to adjust the transfer function of the variable transfer function element circuit to minimize the calibration error signal.

14. The electronic circuit of claim 13, wherein the electronic circuit is configured as a difference amplifier.

15. The electronic circuit of claim 14, wherein the electronic circuit is configured as a high voltage difference amplifier.

16. The electronic circuit of claim 13, wherein the variable transfer function circuit element comprises at least one of a variable resistor, a variable capacitor and a variable current mirror.

17. The electronic circuit of claim 13, wherein the calibration excitation signal generator is configured to generate a signal at an out-of-band frequency.

18. The electronic circuit of claim 17, wherein the calibration excitation signal generator further comprises a switch configured to toggle between first and second reference voltages in response to a clock signal.

19. The electronic circuit of claim 13, wherein the calibration excitation signal generator is configured to generate a calibration excitation signal having a shaped frequency spectrum.

20. The electronic circuit of claim 19, wherein the shaped frequency spectrum is one of random and pseudo random shaping.

21. The electronic circuit of claim 13, wherein the calibration error signal detector comprises a synchronous error detector.

22. The electronic circuit of claim 21, wherein the synchronous error detector comprises:

a latched comparator having first and second inputs and an output;

a capacitor having a first terminal coupled to the input of the latched comparator and a second terminal coupled to the output of the electronic circuit; and

a switch coupled to the first terminal of the capacitor for selectively switching the first terminal of the capacitor to a reference voltage.

23. The electronic circuit of claim 21, wherein the calibration error signal detector further comprises a calibration loop compensation and signal shaping filter coupled between an output of the synchronous error detector and an input of the variable transfer function circuit element.

24. The electronic circuit of claim 23, wherein the calibration loop compensation and signal shaping filter comprises an up/down counter.

25. The electronic circuit of claim 13, wherein at least one of the calibration error signal detector and the filter circuit is configured to operate in accordance with one of a random clock signal, a pseudo-random clock signal, an out-of-band clock signal and a frequency spectrum shaped signal generator.

26. The electronic circuit of claim 13, wherein the variable transfer function circuit element comprises at least one group of fixed resistors which may be selectively switched into and out of one of parallel, series, and combined parallel-series connection with each other to vary the transfer function of the element.

27. The electronic circuit of claim 13, wherein the electronic circuit comprises an analog circuit function.

28. The electronic circuit of claim 13, wherein the electronic circuit comprises a high voltage difference amplifier, the electronic circuit further comprising a pair of external resistors respectively coupled to first and second inputs of the electronic circuit to configure it as a high voltage difference amplifier.

29. A method of calibrating an electronic circuit, the method comprising:

generating a calibration excitation signal;

conducting the calibration excitation signal to a signal path of the electronic circuit;

simultaneously conducting an operating signal of the electronic circuit and the calibration excitation signal on the signal path to responsively generate a calibration error signal on the signal path;

detecting the calibration error signal on the signal path;

evaluating the detected calibration error signal; and

adjusting a variable transfer function circuit element in the signal path in accordance with the evaluation of the detected calibration error signal so as to minimize the calibration error signal.

30. The method of claim 29, wherein generating the calibration excitation signal comprises generating one of a random calibration excitation signal, a pseudo-random calibration excitation signal, an out-of-band calibration excitation signal and a frequency spectrum shaped signal.

31. The method of claim 29, wherein generating the calibration excitation signal comprises a signal generator configured to shape the frequency spectrum of a clock signal.

32. The method of claim 29, wherein detecting a calibration error signal comprises detecting a calibration error signal synchronous with the calibration excitation signal.

33. A high voltage difference amplifier having an instrumentation amplifier with an inverting input coupled to a first external resistor, a noninverting input coupled to

a second external resistor, wherein the first and second external resistors are unmatched external resistors, and an output, the high voltage difference amplifier circuit comprising:

at least one variable transfer function element coupled between a voltage reference node and at least one of the inverting input and the noninverting input of the instrumentation amplifier; and

a calibration excitation signal generator coupled to the voltage reference node for transmitting a calibration excitation signal through the variable transfer function elements to the input of the instrumentation amplifier without interrupting normal operation of the high voltage difference amplifier circuit.

34. The high voltage difference amplifier circuit of claim 31, further comprising a synchronous error detection circuit coupled to the output of the instrumentation amplifier for detecting a calibration error signal..

35. The high voltage difference amplifier circuit of claim 32, further comprising calibration control circuitry coupled between the variable transfer function elements and the synchronous error detection circuit and configured to adjust the variable transfer function elements in response to an error detection signal from the synchronous error detection circuit.